PRECISION RADIAL VELOCITY SPECTROMETER

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CHANGE RECORD

Issue	Date	Section affected	Change Description
0.3	31/7/06		Controller positioned in rack Modify temperature references
0.4	2/8/06		Note added on inter channel cross talk Appendix added with Adrian's technical note
0.5	12/9/06		Comments received from internal reviewer More details given on cold preamp and internal flexis
1.0	14/9/06		Final review before release to Gemini by DWL

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List of Abbreviations

PRVS	Precision Radial Velocity Spectrometer
H2RG	Hawaii-2RG detectors
SNAP	Super Nova Acceleration Probe
H1RG	Hawaii-1RG detectors
VISTA	Visible and Infrared Survey Telescope for Astronomy
CDS	Correlated double sampling
NDR	Non Destructive Read
MICHELLE	Mid Infrared Echelle Spectrometer
WFCAM	UKIRT Wide Field Camera
UKIRT	United Kingdom Infra Red Telescope
ULTRACAM	Ultra-fast, triple-beam CCD camera
FMOS	Fibre-fed near infra red (J & H band) multi-object spectrograph
DAZLE	Dark Ages 'Z' Lyman Explorer
DSP	Digital Signal Processor
ASIC	Application Specific Integrated Circuit
ESO	European Southern Observatory

Definitions

TBD	To Be Defined : a requirement to be developed during the preliminary design stage of the instrument.
TBC	To Be Confirmed : a requirement that is correct with the current design information but requires confirmation during the preliminary design stage of the instrument.
TBR	To Be Reviewed : a requirement specified to meet the PRVS top-level requirements, but which might over-constrain the design.

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1. INTRODUCTION

The detector control system provides the low temperature, high thermal stability, low mechanical flexure and low thermal background environment in which to safely mount and optimally readout the detectors. The PRVS detectors will consist of a mosaic of two Rockwell HAWAII-2RG (H2RG) devices. These detectors will be read out in approximately 1-2 seconds with variable exposure times from 1s to 2000s. Standard noise reduction techniques such as Correlated Double Sampling and Non Destructive Readout sampling will be supported. The detectors will be optimised to have high well depth, good quantum efficiency, good linearity, whilst minimizing read noise, dark current, thermal drift, cross-talk, and cosmetic defects. A Multiple Window Readout Mode will be implemented where typically 10 to 100 windows of approximate sizes of 20x20 pixels will be supported on each detector in the mosaic. A detailed design for the detector control system is presented here, using the SDSU-3 controller. This is the preferred design at this stage of the project life cycle.

2. APPLICABLE AND REFERENCE DOCUMENTS

Reference	Document Title	Document Number	Issue & Date
1	H2RG Technical Documentation		1.1a, 01-08-2003
2	High-speed multiple window readout of Hawaii-1RG detector for a radial velocity experiment - Nagaraja Bezawada and Derek Ives	SPIE 6276	2006
3	The effect of detector cross talk on the radial velocity sensitivity of PRVS – internal memo – Adrian Webster		Version 1, 2006

3. IMAGER DETECTOR SYSTEM

Other detectors considered for this Design Study were the Rockwell HAWAII-2, the Raytheon VIRGO and ORION detectors. However the Multiple Windowed Readout Mode which is an integral part of the instrument design meant that the HAWAII-2RG detector was the only detector of choice for the final design, since it was the only detector capable of performing this readout mode.

Other detector controller options were also considered for this review such as the Rockwell SIDECAR ASIC. The main advantage of operating the ASIC would be if they could be mounted close to the detectors and operated cryogenically. This would then reduce the electrical connectivity required to the outside world and also preclude the user of cryogenics preamplifiers. However the ASIC has still to be proven cryogenically at this time (private communication with Rockwell, July 2006). There are no advantages of using the ASIC devices warm outside the cryostat compared to our chosen solution of SDSU-3 controllers. There would then still be a need for cold preamplifiers and the same number of connections etc. Also the learning curve and lack of support tools excludes their selection at this time.

3.1 HAWAII-2 RG DESCRIPTION

The PRVS detector mosaic will use two, 2048×2048 pixel Rockwell HAWAII-2RG detectors. Each detector has 18 μm square pixels and is mounted in a three-side buttable package. Detailed mechanical dimensions of the H2RG package can be found elsewhere[1]. The minimum separation between the active areas is 2.14 mm. Mounting constraints dictate that the actual minimum separation possible will probably be less than 2.5 mm. The four edge rows and columns of each detector are masked for use as reference pixels, so the light-sensitive area consists of 2040×2040 pixels. Typical performance parameters relevant to the PRVS instrument are given in the table below.

From the table we can see that we require devices with 1.75 um wavelength cut-off material. There are no known issues with using the shorter wavelength cut-off technology. This short wavelength cut-off material has already been proven at Rockwell where it has been developed for the SNAP project and an ESO project. We have also specified the use of all 32 outputs to increase the frame rate and thus the number of non destructive samples per exposure. We will also operate the devices at less than 70 K to ensure the lowest dark current. Typically at 60-70K this has been shown to be less than 0.01 e/pixel/second.

Table 1: Performance Parameters for HAWAII-2RG detectors

Parameter	Specification
Total Pixels	2048×2048
Pixel Pitch	18.0 μm
Fill Factor	> 90%
Outputs	32
Spectral Range	0.9 μm to 1.7 μm
Operating Temperature	40-70 K
Quantum Efficiency @ 77 K	
@ 1.7 μm	> 0.65
@ 1.5 μm	> 0.65
@ 1.0 μm	> 0.65
Charge storage capacity	> 80,000 e
Pixel operability	> 95%
Dark Current @ 70 K (mean)	< 0.01 e/pixel/s
Read noise @ 77 K & 100 kHz	< 15 e/pixel rms (CDS)
Power Dissipation at 100 kHz	< 4 mW

The Hawaii-1RG/2RG readout integrated circuits (multiplexer) offer various features such as selectable outputs, low/ high speed operating modes, simultaneous window access, various reset modes and a variety of clocking modes etc. The multiplexer allows the programming of any desired location and size of window which can then be independently reset or read. This allows implementation of, for example, guide star observations on a sub-window whilst integrating the science observations on the rest of the detector. Several such windows can be accessed in sequence by programming the multiplexer for one window operation at a time. This feature allows the user to define a number of windows around the bright reference spectral lines expected from PRVS across the detector and then be able to read or reset these to avoid saturation of these lines whilst integrating the object spectra on the remainder of the detector. The multiplexer can be configured to provide the window data on a separate output or through one of the standard outputs that are used to read the full frame. This multiple windowing feature with reset/read options is only available on this family of devices from Rockwell and no other manufacturer and therefore means that only it meets the multiple windowing requirements for PRVS. The HAWAII-2RG is a complex device. I discuss the relevant specific complex features that will be implemented for PRVS.

3.1.1 Outputs Pads Configuration

The H2RG has 32 output channels (OutputA/B[0-15]), one reference output (RefOutA/B) and one guide window output (WindowOutA/B). Each output can be configured according to the figure below. Each output is brought out on two pads, A and B. Pad A offers three options; 100 kHz unbuffered, 100 kHz buffered, and 5 MHz unbuffered. Pad B offers the same three options plus the additional configuration for 5 MHz buffered. Two pads are needed because the 5 MHz buffer adds significant capacitance (~ 6 pF) to the line even if disabled. The signals to enable and disable the various options are described in the H2RG Technical Documentation[1].

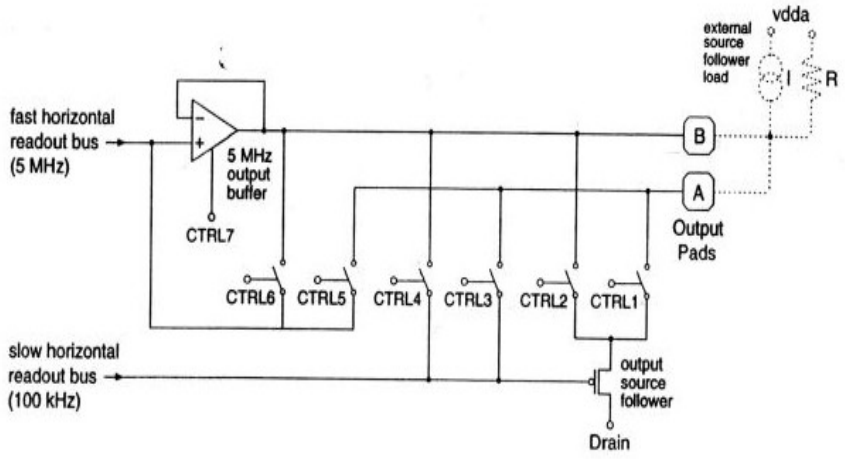


Figure 1 Circuit diagram of various output pad configurations.

3.1.2 Reference Output

Some level of bias stability is required of the detectors. From experience gained with HAWAII-2 detectors which suffered from low frequency banding then it seems sensible to utilize the reference pixel hardware on the H2RG device. The H2RG has a separate reference output for tracking bias variations. This reference output can be configured in different ways. REFMODE in the OutputModeReg register selects whether or not the pixel is treated as a normal pixel. When REFMODE = 0, the pixel is reset at the same time as the upper left (0,0) pixel is reset. Between resets, the pixel node floats and will move slightly due to leakage current in the connected transistor. When REFMODE = 1, the pixel stays in the reset state and is permanently connected to either DSUB (when REFVOLT = 1) or Vreset (when REFVOLT = 0). REFVOLT is a bit in the OutputModeReg register. The circuit diagram for the reference pixels is shown below in Figure 2.

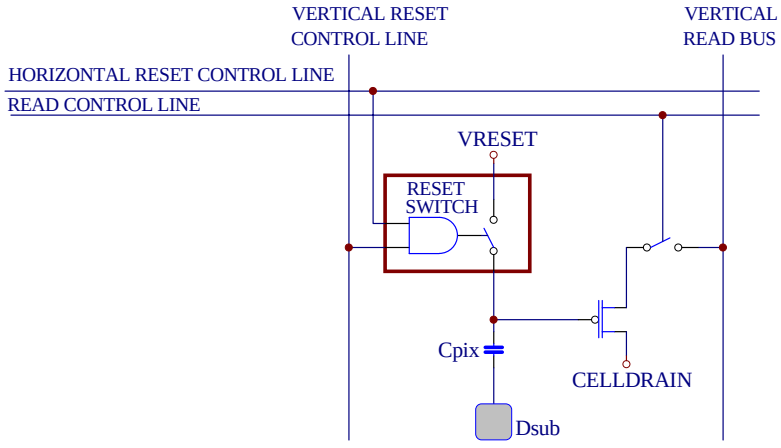


Figure 2 Circuit diagram of the reference pixel.

In our PRVS design we will use a cryogenic differential preamplifier per detector output, 64 such amplifiers in total for the two detectors. Our preamplifier is a differential amplifier design using CMOS TLC2274 op-amps which work reliably at cryogenic temperatures. A circuit schematic for the cryogenic preamplifier design is shown below in Figure 3.

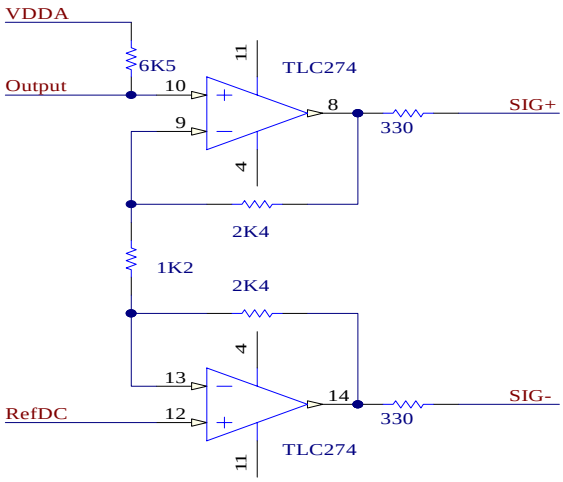


Figure 3 Circuit diagram of cryogenic differential preamplifier.

This circuit has been proven on the VISTA camera system where 256 such preamplifiers are used cryogenically. It has also been used for laboratory evaluation of a HAWAII-1RG detector. The reference input to the differential preamplifier is derived from either the internal detector reference output, *RefDC*, as described above or from an external controller reference voltage. Connecting the reference output in this way will provide some automatic compensation for any minor thermal drifts etc. The reference pixel output can also be taken outside the cryostat to the controller and be sampled and digitized in the same manner as the other detector outputs.

3.1.3 Readout Speed

The H2RG supports two readout speed modes; 100 kHz slow readout and 5 MHz fast readout. The slow readout mode has an advertised read noise of 15 e^- and the fast readout mode has an advertised read noise of 100 e^- . If the 5 MHz read noise is as advertised then this is unsuitable for the PRVS application; the 100 kHz outputs will therefore be used for our design.

The CDS full frame read time using the 100 kHz mode and 32 output amplifiers per H2RG will be typically less than 1.5 s. This means that for longer exposure times of greater than a few hundred seconds we should be able to execute greater than 200 non destructive reads which gives best noise performance. This has been confirmed both by our own in house tests and with other groups. The plot below in Figure 4 shows typical noise versus number of non destructive reads for the H1RG detectors as tested in our laboratory[2].

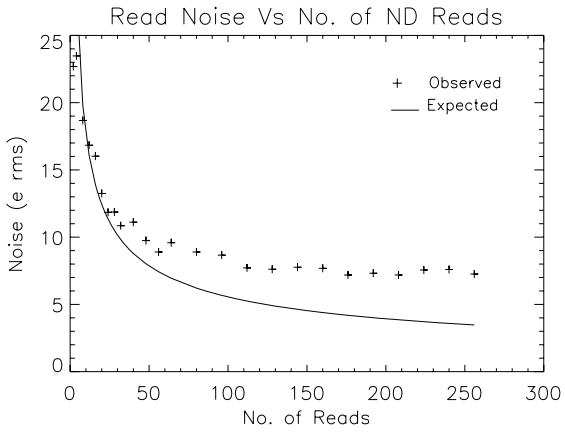


Figure 4 Read noise versus number of non destructive reads

3.1.4 Multiple Windowed Readout Mode

The window mode is enabled by the corresponding bits (VWMEN and HWMEN) in the detector programmable registers. Once the window co-ordinates are programmed and the window mode is enabled, the window data can be immediately accessed. The programming involves resetting the internal registers (main reset) and programming the start and stop registers for the vertical and the horizontal window scan registers. The window mode can then be enabled by the corresponding bits in the MisReg or using the external lines. The window data can either be routed through normal output '7' or through the separate window output. We have confirmed at the UKATC that there are no performance differences between using the window output and the standard outputs, however the addition of two extra video channels to our controller allows sampling of the window through the separate output and also sampling of the reference pixel output. The window can be any size in a rectangular format within the allowed pixel format. A single pixel window can even be defined. Programming for multiple windows is no different to a single window programming. Several or indeed hundreds of windows can be programmed consecutively in a serial sequence to allow a read or reset operation on one window at a time. However for each window it is required to re-program all the internal registers (including registers for selecting number of outputs, speed of operation, selecting buffers etc) when programming the new window co-ordinates in the window start/stop registers. In a test setup on a H1RG performed at the UKATC, up to 32 windows were defined and readout in sequence as shown in the Figure 5 below. In this example, the windows are positioned to map out the word "ATC" on the array. At 100 kHz readout speed of operation, it takes approximately 4.4ms for programming and reading of a 20 x 20 window, of which, in our SDSU-3 controller setup, it requires approximately 100 μs overhead for window programming. For 32 windows we can run at a windowed read rate of approximately 7 Hz.

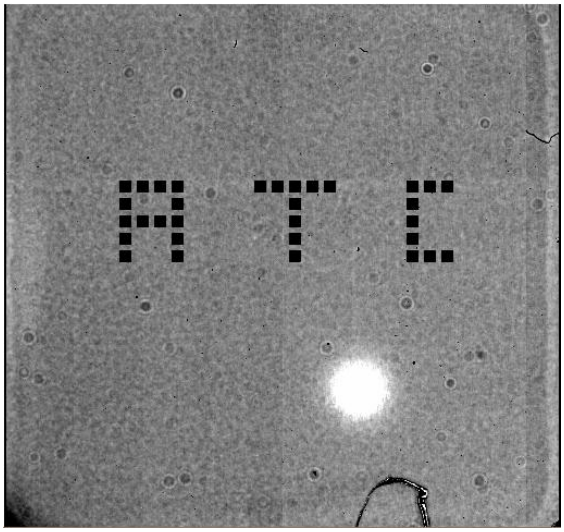


Figure 5 Multiple windowed readout of a HAWAII-1RG detector.

3.1.5 Detector Package

The HAWAII-2RG detector has a hybrid construction consisting of a HgCdTe detector layer deposited on a CdZnTe substrate that is bonded to a HAWAII-2RG multiplexer to form a H2RG Sensor Chip Assembly. The H2RG Sensor Chip Assembly is bonded to a molybdenum package base as shown in the diagram below. Four invar studs screwed into the bottom of this base are used to mount the package in the focal plane on a psuedo-kinematic mount. Normally all four invar studs are used in order to provide symmetric cooling across the detector. The detector is strain relieved by providing a split in the mount plate for the fourth mount stud. Precision-ground molybdenum spacers are used to accurately align the package with the focal plane. A ceramic circuit is attached to one side of the package. This provides wire-bond connections to the Sensor Chip Assembly on its top surface and an external wiring connector and surface-mounted filter components on its bottom surface. There are three variants of the detector packages; a NGST non-ASIC detector package, an ASIC detector package, and a 32-output non-ASIC detector package. The 32-output non-ASIC detector package, shown below, has been designed for ESO and would be our preferred choice for PRVS. Accessing all 32 signal outputs, one reference output, and one guide window output requires a larger connector than can fit on the normal ceramic circuit. A multi-layer ceramic PCB routes the detector signals from the bond pads on top of the detector to a pin grid array behind the detector. This PCB also holds a few filter capacitors for use with the detector biases. One end of a flex is the array of the pin grid sockets and the other end is a high density 92-pin Hirose connector which is then used to make electrical contact with external interfaces. This is shown more clearly in Figure 7 below.

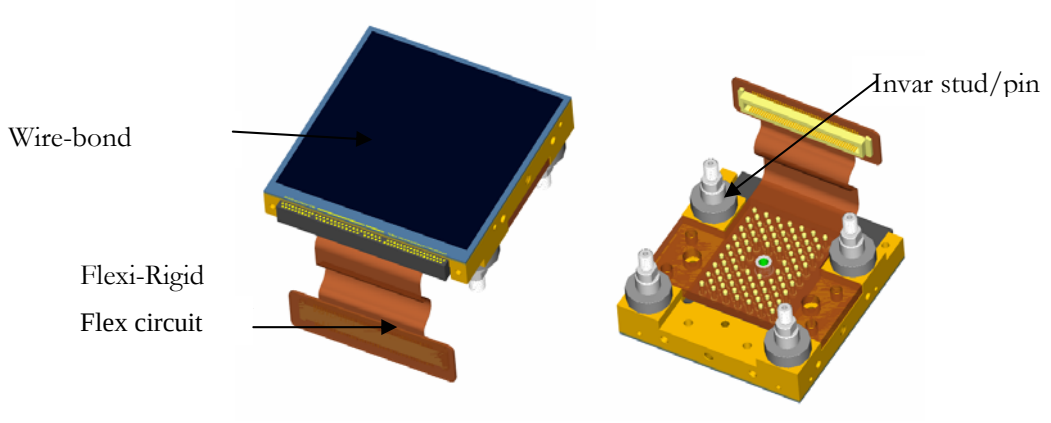


Figure 6: H2RG 32-output non-ASIC (ESO) detector package.

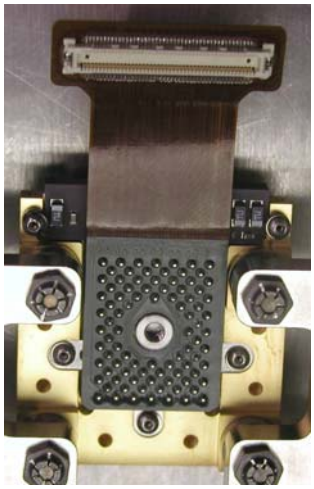


Figure 7: Flexi-rigid detector cable attached to the PGA behind the detector

3.2 FOCAL PLANE ASSEMBLY

The focal plane assembly is the cryogenic subsystem in which the detector mosaic is mounted. It consists of the two detectors, the detector base plate, the detector cold finger, the detector motherboard which house the preamplifiers and conditioning circuitry, the connectors for thermal and electrical control, and the detector housing. The UKATC has many years of experience in the mosaicing of detectors, for example, we built a mosaic with four HAWAII-2 detectors for WFCAM. This was a much more difficult problem to solve than that envisaged for PRVS, because these detectors were packaged in pin grid arrays, were mounted into ZIF sockets and because of the requirements of the faster optical system. We therefore do not foresee any problems in building up a 2 chip mosaic assembly.

3.2.1 Requirements

The requirements for the focal plane assembly will include the following :-

- Flexure at all orientations of the focal plane with respect to the detector housing shall be controlled as required in the x and y directions, where the z direction is normal to the detectors.
- The spacing between the detectors shall be as required. The columns of the detectors can also be aligned if required.
- The focal plane assembly shall shield the detector from, and not generate, background radiation such that the detector dark current requirement can be met.
- The focal plane assembly shall allow the detector temperature to be thermally controlled to ±1 mK between 40 K and 70 K.
- Heat flow in the vicinity of the detector mosaic shall be symmetric to the greatest extent possible in order to minimize temperature gradients within the detectors.
- Cold strap connections shall be made from the back of the detector housing for ease of assembly/disassembly.
- Electrical (both temperature and detector) connections shall be made from the back of the detector housing for ease of assembly/disassembly.
- The focal plane assembly shall be electrically isolated from the rest of the cryostat and connected to detector ground to allow the detector housing to act as a Faraday shield to reduce electrical noise pickup.
- Convenient attachment points shall be provided on the front face of the detector housing for mounting.

3.2.2 Thermal Design

A possible solution for the thermal design is shown in the Figure 8 below. A cold strap connects the cold stage of the cryocooler to the detector housing. The temperature of the detector housing is servo-controlled to 5 K less than the focal plane to a stability of ±0.1 K using the secondary loop of the Lakeshore Model 340 temperature controller. The mass of the detector housing thermally decouples the focal plane from temperature fluctuations of the cryocooler. A cold strap connects the detector housing to the focal plane mounting plate. The temperature of the focal plane mounting plate is set to between 40 K and 70 K and is servo-controlled to milli-Kelvin stability using the primary loop of the Lakeshore Model 340 temperature controller. This design will also ensure that the detectors can never be cooled down or warmed up at a rate any greater than 0.5K/minute. This ensures that thermal stresses are minimised in the detectors.

3.3 THERMAL CONTROL

The detector thermal control system must regulate the temperature of the detector to milli-Kelvin stability in the range of 40-70 K to ensure low thermal drift and to minimize any differential thermal contraction of the detectors themselves. A Lake Shore, Model 340 temperature controller coupled with a Cernox CX-1080-LR temperature sensor will be used to achieve this requirement. This sensor is preferred to a forward biased diode to ensure that transients induced by clock pickup are not rectified and thus have no impact on the slow thermal loop control. The specification and performance of this combination are described in the table of Figure 9 below. The same combination has been successfully used on other instruments to control the temperature of detectors to milli-Kelvin accuracy. The heater resistor should be located so that heat flow between the cooling power and the heater is minimized. This requires that it be in close thermal contact with the cooling power, and if possible that it be mounted by the same screw that holds the cooling strap. The heater resistor should also have low thermal resistance and thermal time lag to allow the temperature control to react quickly to temperature disturbances.

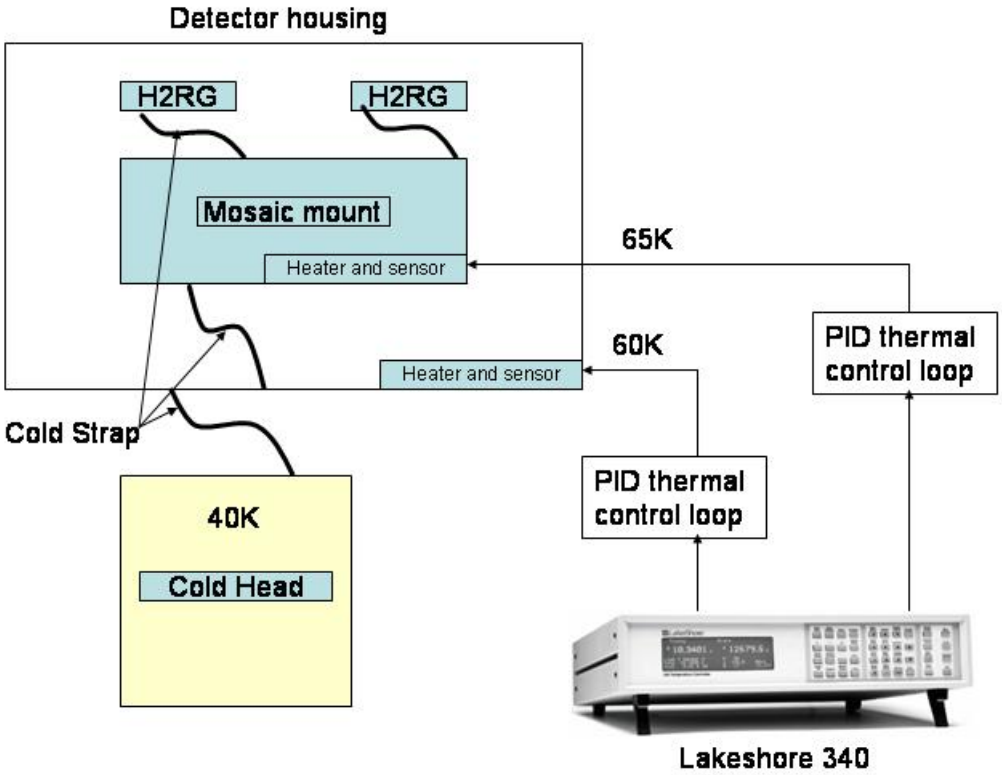


Figure 8 Detector assembly thermal design.

Sensor Type	Cernox (CX1050)
Temperature Coefficient	Negative
Sensor Units	Ohms
Input Range	10 ohm to 300 kohm
Sensor Excitation (constant current)	10 mV max (10 current settings from 30 nA-1 mA)
Temperature Range	10-300 K
Standard Curve	Requires Sensor Calibration from manufacturer
Measurement Resolution:	1.3 mK at 77 K, better at lower temperatures
Temperature accuracy (includes calibration and electronics accuracy)	±84 mK at 77 K
Control Stability	±2 mK at 77 K, better at lower temperatures

Figure 9: Lake Shore Model 340 Temperature Controller and Cernox Performance Data.

3.3.1 Electrical Isolation

The focal plane assembly will be electrically isolated from the cryostat and tied to detector ground. The detector housing then acts as a Faraday shield to reduce electro-magnetic interference. This configuration has been used successfully in the MICHELLE and WFCAM detector systems, built by the UKATC for UKIRT.

3.4 DETECTOR WIRING

The detector wiring consists of the focal plane motherboard in the focal plane assembly, the flex circuits and cables that connect the focal plane motherboard to the cryostat hermetic connectors, and the cryostat hermetic connectors.

3.4.1 Focal Plane Motherboard

The focal plane motherboard provides connections to the two H2RG detectors. It is located in the lower section of the detector housing to prevent locally generated heat, glow, and electrical noise affecting detector performance. The focal plane motherboard is a flexi-rigid printed circuit board. The flexible portions pass through light-tight labyrinths into the low background section of the detector housing and mate with the connectors on the detector packages. The rigid portion of the focal plane motherboard supports surface-mounted filtering components, external connectors, and the 64 differential preamplifier circuits for all the required detector output stages. High-density micro-D sub-miniature connectors provide external connections. Figure 10 below shows the compact 34-channel preamplifier board which provides biases decoupling, over-voltage protection and 34-differential preamplifiers (32 readouts, reference and window outputs) as designed for use with the HAWAII-2RG detector in the ESO KMOS instrument (information supplied by Reinhold Dorn at ESO). The two split flexes carry biases and clocks in one and video signals on the other. ESO uses an additional flex cable to connect to the 92-pin Hirose connector to the D-type connector shown in the figure. We will use this exact design if possible.

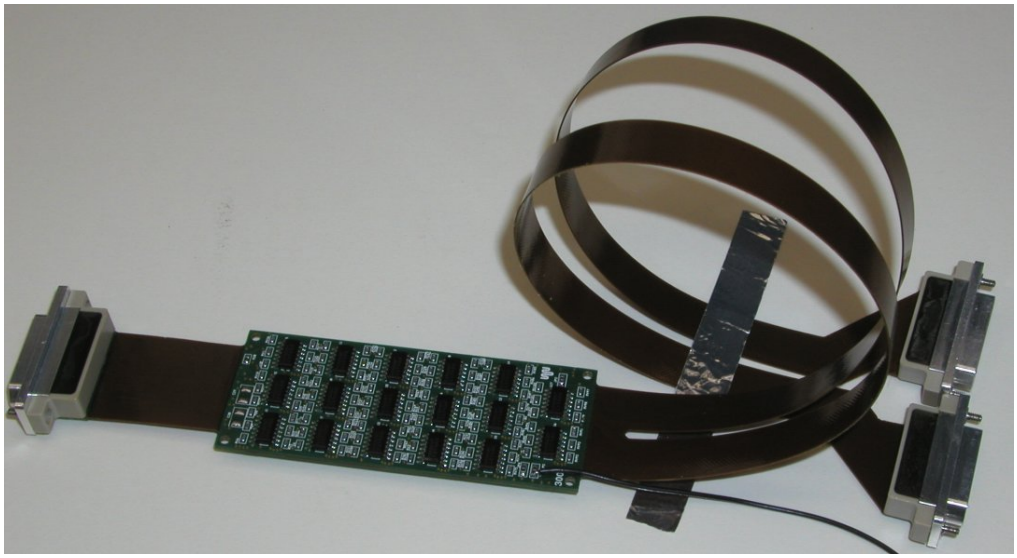


Figure 10: ESO KMOS cold preamplifier and flexi rigid cable system

3.4.2 Cryostat Wiring

The cryostat wiring connects the focal plane motherboard to the cryostat hermetic connectors. This will also typically consist of flexi circuits. An example of such a circuit as used on WFCAM at UKIRT is shown below in Figure 11. The use of flexi-rigid circuits ensures a very high level of build quality. In this example the flexi-rigid was used to connect an array to a hermetic 100 way connector. The flex circuits will be clamped to the warm vacuum jacket near the hermetic connectors to stop moisture condensing on the hermetic connectors outside the cryostat. They will be clamped at the radiation shield to shunt the main heat load to the cold work surface plate. Then they will be clamped to the detector housing stabilizing the wiring temperature before connection to the focal plane motherboard. This will eliminate temperature gradients across the detectors due to variable heat flow through their wiring. Care will be

exercised to match the electrical lengths of pairs and to match the impedances of all cables, flex circuit tracks, and connectors to achieve good transmission line performance.

Figure 11: WFCAM flexi-rigid cable example.

3.4.3 Hermetic Connectors

PRVS will use standard 100 pin, circular hermetic connectors with PCB solder pins for ease of soldering to flex circuits with one connector required per detector for a total of two.

3.5 DETECTOR CONTROLLER REQUIREMENTS

The system will offer the following minimum set of requirements :

- Correlated double sampling, Non destructive and Fowler sampling (1 to 512 samples) read out methods shall be supported.
- Integration times from 1 s to 5,000 s shall be supported.
- Coaddition of between 1 and 1000 data frames shall be supported before the result is transferred to the storage area.
- An idle mode shall be supported whereby the detectors are continuously readout or reset to maintain thermal stability and to prevent them saturating.
- Multiple Windowed Readout Mode, where many windows are readout consecutively, either destructively or non destructively and interleaved with full frame non destructive readouts.

3.6 SDSU-3 DETECTOR CONTROLLER

Our design for the detector control system is based on the San Diego State University SDSU-3, also know as the "Leach" or AstroCam controller. This is an attractive option because both the UKATC and Gemini have extensive experience designing and operating detector systems based on this controller. The UKATC have built many instruments over the years based on SDSU controller technology, for example, WFCAM for UKIRT, ULTRACAM for the VLTs at ESO, FMOS for SUBARU and DAZLE for ESO.

3.6.1 Number of Controllers and Specification

We have considered the options of using one controller per detector and also using one controller to drive and read out both detectors. There are advantages and disadvantages with both options. With the single controller option then the maximum number of video channels we can operate is 64. This means that we will not be able to use the reference outputs on the detectors. Also the controller housing would be fully populated, not allowing room for possible future expansion or upgrades. It is also likely that the SDSU power supply would not be sufficient to power all 64 channels and preamplifiers and would therefore mean a redesign of the "off-the-shelf" SDSU controller power supply. There are some advantages to this design approach in terms of the interleaved readout and the DSP code required to implement it, however there are no space constraints and the extra cost for two controllers rather than one controller to drive two detectors is minimal in the context of the overall instrument cost.
With the two controller solution, one per detector, then we could quite easily accommodate 34 video channels per controller, allowing for both the window and reference outputs as well. Space would be available in the chassis for extra boards if required and the standard power supply will easily accommodate both the controller and its associated 34 channel cryogenic preamplifier circuitry. We have confirmed this already with an analysis and build for WFCAM where we powered a 32 channel system, 32 external preamplifiers and a Low Voltage Differential System (LVDS) clock receiver system. With this design we would have to synchronise the readout of the controllers to ensure that there is no clock coupling between detectors. However we have already successfully synchronized four of these controllers on the WFCAM project. This option is slightly more expensive because an extra chassis, power supply, timing board and PCI board would be required. I assume for now that our preferred option is the controller per detector option.

The SDSU-3 detector controller housings will be mounted in a rack, within 1 metre of the hermetic connectors on the vacuum jacket. If this close positioning is not possible then the housings will be mounted directly off the vacuum housing itself. This close proximity to the detector minimizes wiring capacitance and so reduces the required drive currents. We have experience of driving long cables between detector and controllers with WFCAM, where we were able to obtain detector limited noise performance over long cable runs (>8 metres).

A single SDSU-3 detector controller would be used to drive one of the H2RG detectors and consist of the following components as described here and shown below :

- Five SDSU 8 Channel IR Video Processor Boards configured for H2RG devices. Each board has eight video processing channels and seven programmable bias generators. The video processing channels have programmable bandwidth and gain.
- One modified SDSU IR Clock Driver Board. Each board provides 24 clock/bias generators in two banks of 12 clocks/biases.
- One Fiber-Optic Timing Board. This board provides the timing sequencer and the communication hub for the other boards.
- One SDSU Power Controller, one SDSU 12-slot back plane, and one SDSU enclosed water cooled housing.
- One 12.5 Mpixel/s SDSU PCI interface board. This board plugs into the PCI slot on a PC motherboard. It provides the fiber-optic communication interface between the SDSU-3 detector controller and the PC.

3.6.2 Functional Description

The following sections give a detailed overview of the controller electronics required to operate the chosen detector types.

3.6.3 Communications Interface

Communication with each of the SDSU-3 detector controllers is via the SDSU 12.5 Mpixel/s PCI interface board mounted in a 19 inch rack mounted PC. A fiber-optic link connects the SDSU PCI interface board to the timing board in the SDSU detector controller. One PC and PCI board would be required per controller. A fault tolerant protocol developed at UKATC and used successfully on WFCAM and ULTRACAM is used for the communication between PC and SDSU controller.

3.6.4 Timing Sequencer

A Motorola DSP56303 Digital Signal Processor (DSP) is at the heart of the timing board. This DSP has a 100 MHz clock and runs at 10 ns per instruction but only at 40 ns per waveform clock cycle. It controls the setting of clocks, biases, video offsets, and power supply voltages. It also controls the sequencing of clocks and analog switches on the video boards whilst reading out the detector. It also controls the use of clocks to provide the serial communication path to set the programmable registers in the H2RG multiplexers. Finally it controls the transfer of detector data from the ADCs on the video boards via the fiber-optic link.

3.6.5 Bias Generation

Bias generation is supplied from the standard bias circuitry on the IR video boards. The components are modified slightly to match the H2RG detector and to offer improved gain and bias stability using higher specification resistors.

3.6.6 Clock Drivers

One SDSU clock driver board provide the clocks required to drive a detector. Each clock driver board has the capability to drive two banks of 12 clocks. However in our design the H2RG will be driven by one dedicated bank, the other bank will then be configured as the serial interface to the detector to allowing programming of the detector registers for window setup etc.

3.6.7 Imager Video Chain

Five video boards provide 40 video channels to digitize the 34 output signals from each H2RG detector. The input stages and gain settings of the video stages will be matched to the cryogenic differential preamplifiers to give best noise performance and full dynamic range. This means that we have a full differential system from detector output to digitization within the controller which will improve bias stability and reduce noise pickup in the cabling.

A block diagram, Figure 12, is shown below which shows all the main electrical components required to readout the two H2RG detectors. The controllers themselves would be mounted on or close to the cryostat in a rack to ensure that they are close to the hermetic connectors and that the cable lengths are minimal. The power supplies for the controllers will also be mounted in the same rack. The PCs can be mounted anywhere within a few hundred metres of the controllers since the only connection between controller and PC is via a duplex fibre optic link, however they will also probably be mounted in the same rack.

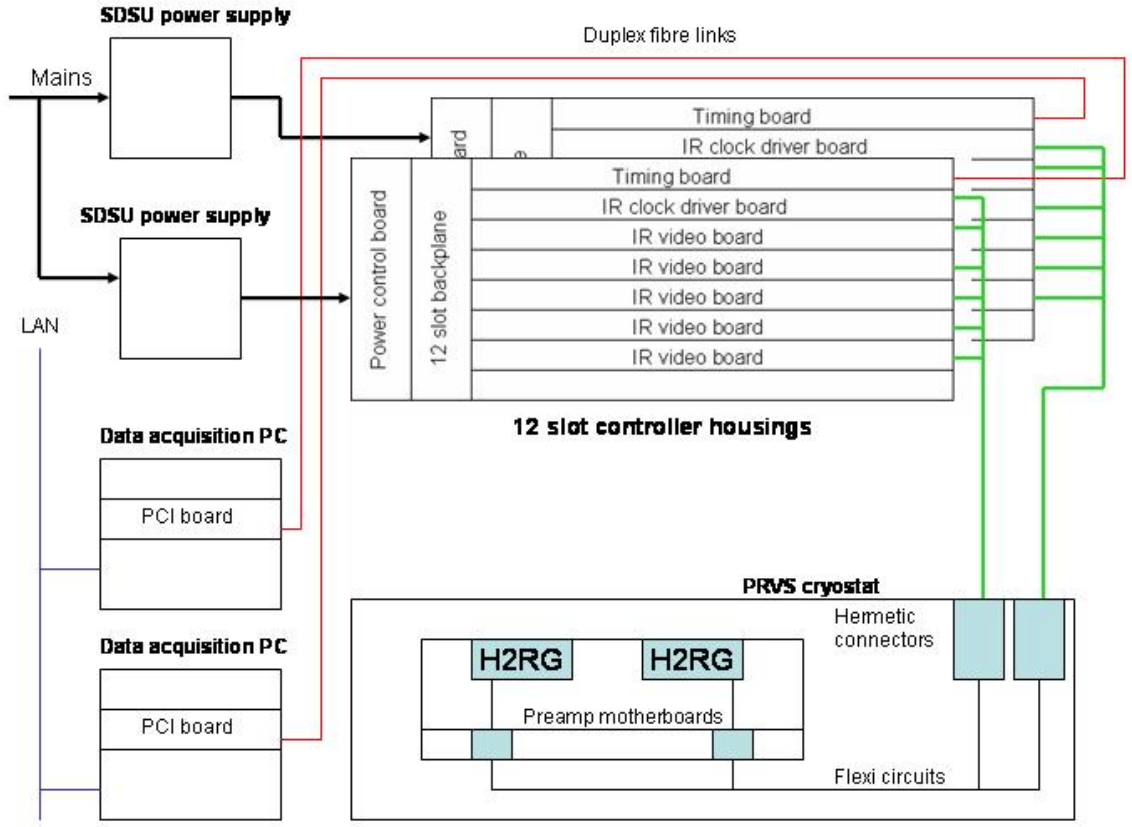


Figure 12: Block diagram of SDSU-3 detector controller design for PRVS.

3.7 DETECTOR READOUT SEQUENCING

It is a requirement of the system that multiple windows are read out from the detectors in an interleaved fashion whilst doing full frame non destructive readouts. This is a complex process as the windows will be "randomly" positioned throughout a detector. They will also lie on different positions on the two detectors. Likewise some of the windows will be required to be readout destructively because they are imaging very bright lines whereas others may be required to be read out non-destructively. It must also be remembered that the windows themselves can only be readout sequentially. I have made the following assumptions to simplify the interleaved read out process to develop one particular read out algorithm which would meet our requirements:-

- There will be a maximum of 256 windows at random positions on a particular detector
- There will therefore be a total of 512 windows for the two detectors.
- All windows will be of equal size.
- Any window can be destructively or non destructively readout.
- To aid DSP programming then there will be the same number of enabled and destructive/non destructive windows on each detector – this is also important for synchronization purposes. This means that, for example, if only 32 windows were defined on one detector but 64 were required on the other then we should in effect define 64 windows each on both detectors. This option ensures that windows are readout in parallel on the two controllers. An alternative method would be to read all the windows out on one detector then read all the windows out on the other detector. In this case different numbers of windows would be allowed on each detector. This

function could be implemented by passing synchronization signals between controllers. However the frame rate would be twice as slow as the first option.

From the testing we have performed on a H1RG detector we know that it is possible to read out 128 windows of size 20x20 pixels at approximately 2 Hz.

The controllers would then require the following parameters to read out all the windows, interleaved with full frame read outs.

- X-Start and Y-Start position for each of the windows.
- Whether a particular window is to be read out destructively or non-destructively.
- A fixed integration time between the readout of each window.
- The number of times to readout all the windows before reading out a full frame.
- The number of times to repeat the whole windowed readout and full frame readout sequence.

A possible algorithm to implement the windowed/full frame interleaved readout is given below in Figure 13.

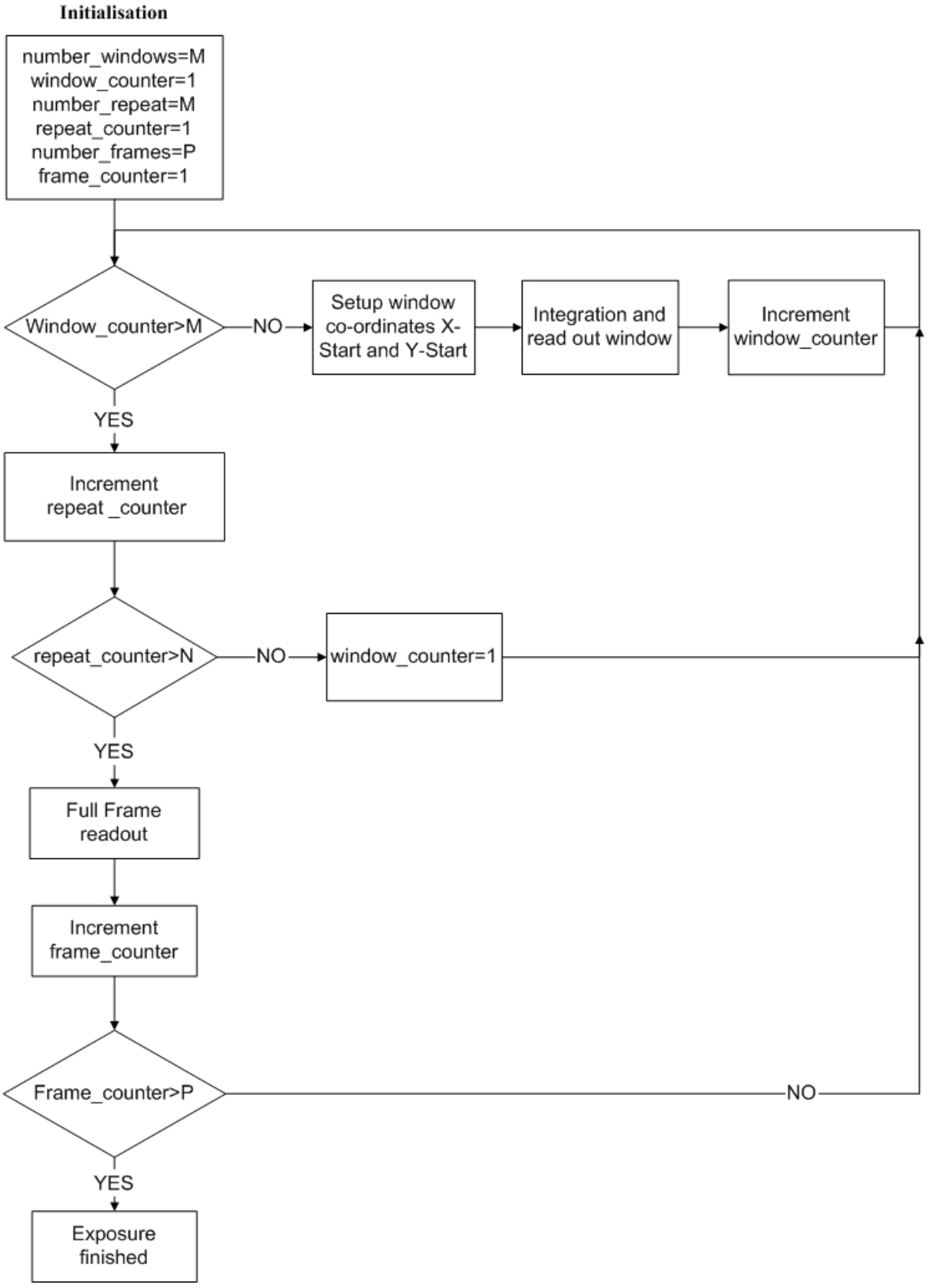


Figure 13: Flow chart for windowed/full frame interleaved read out

3.8 DETECTOR ISSUES WHICH MAY AFFECT PRVS EXPERIMENT

3.8.1 Input Noise

The detector controller should have an input noise that is small relative to the detector read noise of approximately 15 e^-. The video chain noise with a 1 kΩ input load is expected from past experience to be less than 3 e^- . Consequently, controller noise should add less than 2% to the detector read noise.

3.8.2 Bias and Gain Drifts

Temperature variations in the detector controller can cause bias and gain variations. These will be reduced by stabilizing the controllers' housing temperature to ±2 K using water cooling if mounted on the vacuum vessel or by being positioned in a thermally controlled rack. The reference outputs will also be used to track and electrically subtract drift as described earlier. The reference output will be fed into the differential preamplifiers but can also be sampled using an extra video channel. The outer four rows and columns of reference pixels will be sampled. These can be subtracted during data reduction to attenuate *1/f* noise at periods greater than one row read time.

The temporal stability of a H1RG detector used with our preamplifier design and SDSU-3 controller has been tested at the UKATC[2]. I briefly report on it here to indicate expected performance. In order to investigate the flat-field stability of the detector, co-adds of many identical flats were used to improve the flat-field accuracy. A window of 200 x 200 pixels was used and a sequence of 2000 CDS frames were obtained, each flat field having ~15k e^- signal from a K band setup. A first set of several co-adds from different numbers of frames (e.g. using the first 10 frames, first 20 frames, all the way up to using the 1000 frames) was obtained from the first 1000 frames. Similarly a second set of co-adds was created from the later 1000 CDS frames. Every co-added frame in the first set was divided by the corresponding co-added frame in the second set and the standard deviation in the resultant frame was plotted against the number of frames in a given co-add as shown in the Figure 13 below. For a comparison, $1/\sqrt{n}$ (n being the number of frames in a given co-add) is also plotted in the same graph. As can be seen from the plot, the flat-field stability is ~ 0.05% for co-adds of approximately $15 \times 10^6 e^-$ of signal.

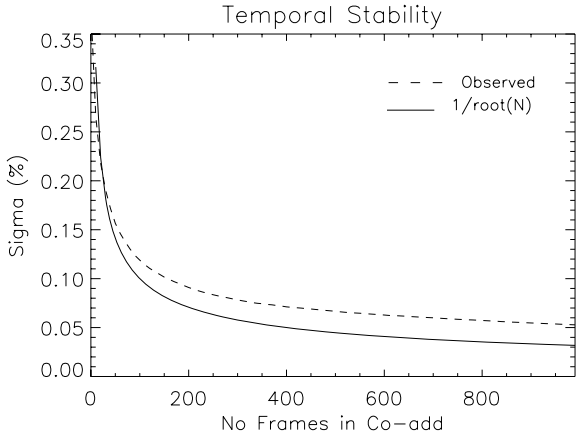


Figure 14: Temporal stability from numbers of co-adds for H1RG detector + SDSU-3 controller

3.8.3 Persistence

Persistence is a feature of these detector types and is an issue for PRVS. It has been suggested that it may vary across the same detector types, that is, one H2RG detector may be worse than another H2RG. It seems prudent that if this is the case then when placing the order for H2RG detectors, we specify that the detectors are tested for persistence and that the best performing devices are chosen, all other options being equal. Persistence has been investigated using our H1RG device. It has been shown that the amount of persistence signal is proportional to the integration time of the latency image producing the persistence. It appears that there is no significant increase in the persistence signal with the signal level until just about the saturation point of the detector is reached. The figure below shows the decay of the persistence signal current measured from the 15s dark integrations taken at the UKATC with a H1RG, following the exposure to various fluence levels.

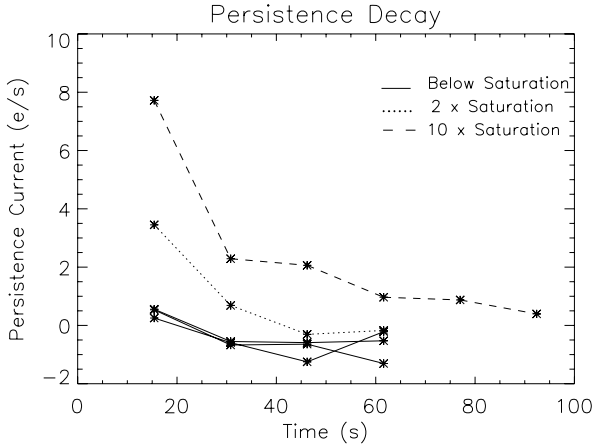
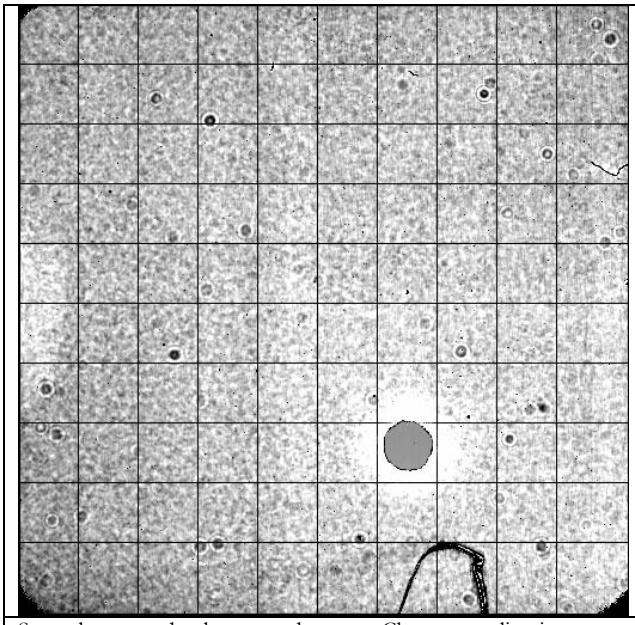


Figure 15: Persistence signal decay

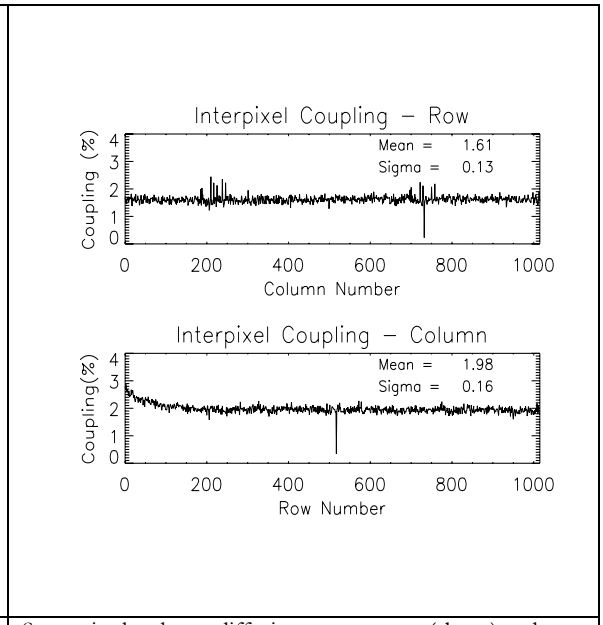
It seems prudent therefore to ensure that the detectors are not saturated, if at all possible. There also have been reports that reducing the detector temperature may reduce the persistence problem. We will therefore allow for operation of the detector down to 40K. We are in contact with the SNAP group at Caltech and will implement whatever recommendations they may make for optimal detector performance.

3.8.4 Inter pixel capacitance issues for PRVS

A model developed at the UKATC on the effect of the inter-pixel capacitance on the radial velocity sensitivity[3] showed that whilst symmetrical charge coupling to neighbouring rows/columns does not induce any velocity shifts, the variation in charge coupling can cause variation in the velocity error. To measure the capacitive coupling across the detector, the window feature was used to define a window of one full row or one column to investigate the extent and the variation of the interpixel capacitive coupling. A few rows and columns across the array are kept under reset whilst integrating the remaining pixels. This allowed us to measure, from a normalized difference frame, the extent and the scatter of the capacitive coupling in a row or column and its symmetry from its neighbouring rows or columns. The scatter is estimated to be around 0.1 – 0.15% of the values of the mean of the capacitive coupling as shown in the figure below. Both columns and rows showed symmetrical capacitive coupling across the array which is an important result for PRVS.



Several rows and columns under reset. Charge coupling is symmetric across the array.



Scatter in the charge diffusion across a row (above) and a column (below)

Figure 16: Inter-pixel capacitance

The effect of the inter pixel capacitive coupling on the Full Width Half Maximum has also been modelled as shown in the figure below. We see, for example, that 2.5% of capacitive coupling from a pixel to its nearest neighbour changes the full width half maximum by a factor of 1.37.

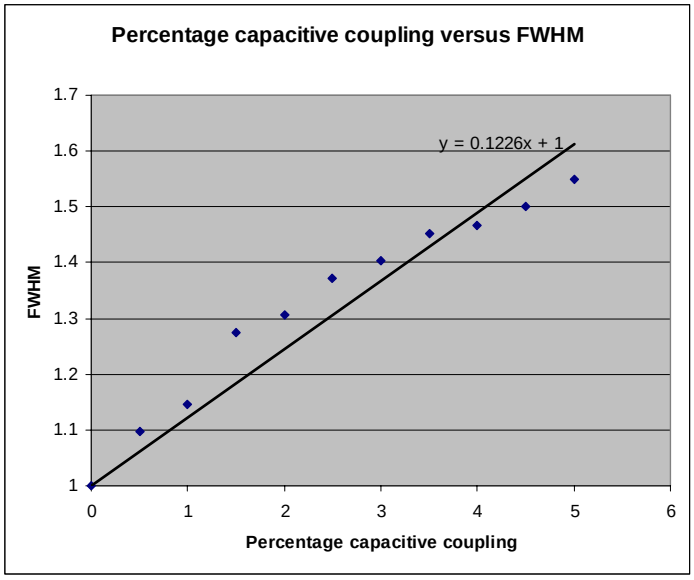


Figure 17: Inter-pixel capacitance effect on FWHM

3.8.5 Inter channel crosstalk

On HAWAII-3 detectors we had noticed that there was coupling between outputs on the same detector which was not associated with the controller but the detector itself. We set out to check if this was also a feature of the H1RG detector as well. In our test setup, the detector was read through two outputs each

handling 512 columns x 1024 rows. A small blackbody aperture was imaged onto one side of the detector which read through channel 1. The signal in the channel 2 was then investigated for the resulting electrical cross-talk. As shown in the table below, the cross-talk in the channel 2 is proportional to the signal in the channel 1. The cross-talk of the SDSU-3, 8 channel controller video boards was measured to be ~0.002% between neighbouring channels. We therefore surmise that the measured crosstalk is a function of the detector itself or the common biases to the detector outputs. Efforts will be made to isolate the source of this cross-talk, for example, by providing separate low impedance output source bias supplies for the two outputs. We intend to carry out this measurement as soon as possible to confirm the source of inter channel cross talk.

Signal level in Channel-1	Cross-talk in Channel-2 (%)
Full well	0.18
¾ Full well	0.18
½ Full well	0.14
¼ Full well	0.08

Table 2: Electrical cross-talk between the two readout channels

3.9 GROUNDING PLAN

The diagram below shows the preliminary detector grounding system. Close attention will be paid to the detector grounding and shielding to achieve the required low noise performance of the detectors. The PRVS cryostat forms the primary shield around the detector. It may not be practical to completely electrically isolate the cryostat from the telescope and mains grounds and ground the cryostat only through the detector controller. Instead, the cryostat will likely be grounded to the telescope. The telescope ground is reported to be a noisy ground so is not ideal for detector grounding purposes. Consequently, our PRVS design will also use an internal detector shield that is insulated and electrically isolated from the cryostat. Ideally, this internal shield would completely enclose the detectors, focal plane, and the cryostat wiring and be connected to the detector controller ground. An approximation to this ideal will be achieved.

The detector focal plane assembly will be electrically isolated from its surroundings and will be connected electrically to detector ground. The cryostat wiring will be shielded by running ground tracks between each signal line, by placing ground planes on the top and bottom of flex circuits, and by shielding all cables. The detector controller grounding scheme is based on making the video boards the star point, and radiating short ground wires from it to the clock board, bias boards, the detector controller chassis, and detector ground. The star point is ultimately attached to Gemini's quiet instrument ground.

Care will be taken so that motors, microswitches, cryocooler lines, cryocooler drives, cables, and mechanical couplings do not ground the cryostat. This would cause multiple ground loops through the instrument.

The cryocooler radiates a strong magnetic field. The intensity and extent of this magnetic field are known. The detector controller, focal plane assembly, and cryostat wiring will be kept out of this field as much as possible. Otherwise, magnetic shielding of these components will be required. The radiation from the cryocooler is directional so care will be exercised when orienting the cryocooler head with respect to the detector controller. The detector controller is housed in a sealed aluminium box and therefore has good electrical (but not necessary good magnetic) shielding. Noisy cables will be routed so that they are as far as practical away from the detector controller. Local motors (steppers) will be powered down when not driving. Motor leads will be shielded and the shields only broken at the cryostat wall.

3.9.1 Shielding Philosophy

It is very important to properly design the grounding and shielding to obtain reliable operation and the best noise performance. As far as possible the following rules will be adhered to:

1. Shielded coax or twisted pair cable will be used to interconnect components. The shields of these cables will only be connected at one end to avoid ground loops. This is standard practice and has been used for many years at the UKATC.
2. Electrically noisy components and signals will be kept away from low level sensitive ones, and ground shields will be placed in between. The detector controllers will be mounted on or close to the cryostat, and kept away from other noisy sources which will be mounted in another enclosure.
3. Noisy grounds will be kept separate from low-level electronics grounds. Several grounds will be used, and these will be connected at one star point. The first ground will be a hardware ground used for mechanical enclosures, chassis, racks, and so on. The second will be a noisy ground used for relays, and motors. The third will be a digital ground, and the last will be a quiet analogue ground. The AC power ground will be connected to the hardware ground. This grounding configuration is shown below in Figure 17.

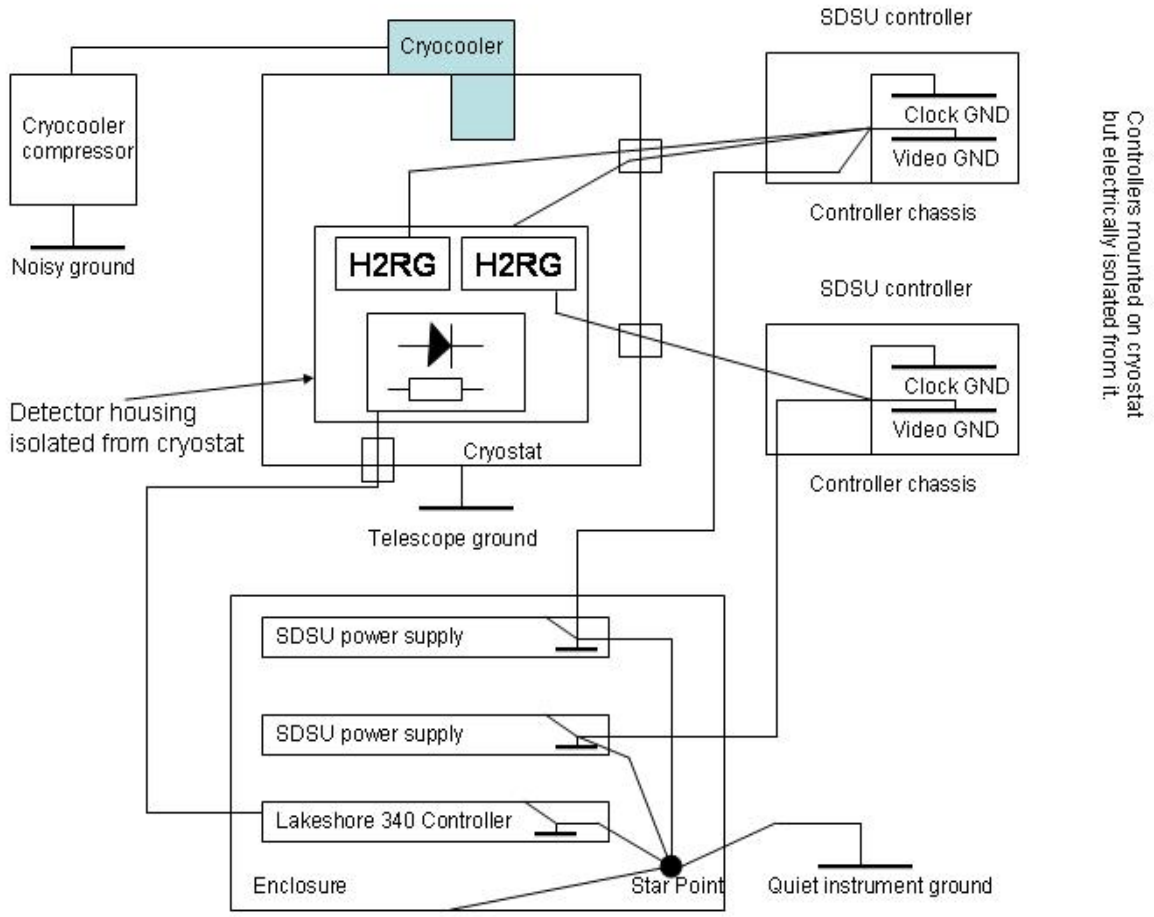


Figure 18: Detector grounding system.